METHOD FOR MANUFACTURING A RECLAIMABLE TEST PATTERN WAFER FOR CMP APPLICATIONS

ABSTRACT OF THE DISCLOSURE

In a method for manufacturing a test pattern wafer, a silicon substrate is provided. A sacrificial oxide layer is deposited over the silicon substrate, and simulated transistor structure test features are fabricated into and on the sacrificial oxide layer. Chemical mechanical polishing characterization is performed using the test pattern wafer which provides data for the characterization of the chemical mechanical polishing. The sacrificial oxide layer is then stripped along with the simulated transistor structure test features, allowing the silicon substrate to be reclaimed and to be used in the fabrication of subsequent test pattern wafers.